AMENDMENTS TO THE SPECIFICATION

On page 1, please amend the paragraph entitled "RELATED APPLICATIONS" as follows:

This present application is related to concurrently filed, commonly assigned U.S. Patent Application Serial No. ~~[Attorney Docket No. 10011125-1]~~ 09/853,951, entitled "SYSTEM OF AND METHOD FOR MEMORY ARBITRATION USING MULTIPLE QUEUES," abandoned, the disclosure of which is hereby incorporated herein by reference.

Please amend the paragraph beginning on page 9, at line 23, as follows:

FIGURE 11 is a diagram of an example of an embodiment of the present invention; and

Please delete the following paragraph beginning at page 9, line 24:

~~FIGURES 12A and 12B are schematic diagrams of logic circuits implementing the counter mask of FIGURE 11 for bit [0] and bit [4] respectively;~~

Please delete the following paragraph beginning at page 10, line 1:

~~FIGURE 13 is a schematic diagram of a logic circuit used to generate the counter mask of FIGURE 11; and~~

Please amend the paragraph beginning at page 10, line 3, as follows:

FIGURE ~~14~~ 12 is a flow chart depicting the generation of a dependency.

Please amend the paragraph beginning at page 22, line 15, as follows:

~~FIGURES 12A and 12B show methods for generating counter mask 1102 values.~~ Counter mask 1102 is generated from the counter value using combinational logic. As shown in Table 1, for each counter value a different counter mask will be generated. Using an eight entry queue with its associated CAMs will require eight different counter values.

Please amend the paragraph beginning at page 23, line 4, as follows:

Masked match bits 1103 is determined by ANDing duplicate match bits 1101 and counter mask 1102. As shown in FIGURE 11, starting from rightmost bit (0) only bits 4 and 10 contain a "1" in both duplicate match bits 1101 and counter mask 1102.

Please amend the paragraph beginning at page 23, line 7, as follows:

~~FIGURE 13 shows a~~ A preferred implementation of generating clear mask 1104 can be implemented using circuitry similar to the circuitry described with reference to FIGURE 10. Bit [0] ~~1301~~ of clear mask 903 is 0. In this example, bit [0] of masked bits 1103 is inputted ~~at reference number 1302~~ to an ORing function which results in bit [1] of clear mask 1104 also being 0. The succeeding bits of clear mask 903 remain at 0 until a bit of masked match bits 1103 is equal to 1. Once this occurs the corresponding bit of the clear mask are equal to one. In a preferred embodiment, the bits of clear mask 1104 remaining after bits in counter mask 1102 transition from 1 to 0 do not need to be determined, but are preferably all set to 1.

Please amend the paragraph beginning at page 23, line 17, as follows:

FIGURE ~~14~~ 12 shows a flow chart which described the steps associated with the identification of the dependency of FIGURE 11. In Step 1401 the original match bits are received and used to generate the duplicate match value. In Step 1402 the counter value is used to generate the counter mask. The counter mask may be generated in advance as a function of the various possible counter values. In Step 1403 masked match bits 1103 are generated by ANDing duplicate match bits 1101 with counter mask 1102. In Step 1404 clear mask 1104 is generated ~~in accordance with FIGURE 13~~. In Step 1405 Applied Masked 1105 is generated by inverting clear mask 1104 and ANDing the resulting values with masked match bits 1103. The dependency is then determined in Step 1406 by ORing the first eight bits, in our example, with the second set of eight bits.